IN THE CLAIMS

Please amend the claims as shown in the following detailed claim listing. The detailed claim listing is intended to reflect the amendment of previously pending claims 1, 2, 9, 14, 15, 19, 20, 21, and 22, and the addition of new claims 24-25. The specific amendments to individual claims are detailed in the following detailed claim listing.

1. (Currently Amended) An apparatus comprising:

a memory device having a memory device input data bus including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a first repair router input data bus including a least significant bit and a plurality of non-least significant bits, and a first repair router output data bus coupled to the memory device input data bus, the first repair router having internal routing circuitry to route any of the plurality of non-least significant bits of the first repair router input data bus to the least significant bit of the memory device input data bus and to discard the least significant bit of the first repair router input data bus.

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2. (Currently Amended) The apparatus of claim 1 wherein:

the plurality of non-least significant bits of the memory device input data bus includes a next-to-least significant bit; and

the first repair router further includes additional repair routing circuitry to route any of the non-least significant bits of the first repair router input data bus to the next-to-least significant bit of the memory device input data bus.

3. (Original) The apparatus of claim 1 wherein the memory device includes a memory device output data bus including a least significant bit and a plurality of non-least significant bits, the apparatus further comprising:

a second repair router having a second repair router input data bus coupled to the memory device output data bus, and having a second repair router output data bus including a least significant bit and a plurality of non-least significant bits, the second repair router having internal

routing circuitry to route the least significant bit of the memory device output data bus to any of the plurality of non-least significant bits of the second repair router output data bus.

4. (Original) The apparatus of claim 3 wherein the memory device includes a plurality of address ranges, and the first and second repair routers include address decoding circuitry to decode each of the plurality of address ranges.

5. (Original) The apparatus of claim 4 wherein the memory device includes two address ranges defined by a state of a most significant address bit.

6. (Original) The apparatus of claim 3 further comprising a display device coupled to the second repair router output data bus.

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7. (Previously Amended) The apparatus of claim 6 wherein the display device is a color display device, and the memory device and first and second repair routers influence a first color of the color display device, the apparatus further comprising:

a second memory device; and

a second pair of repair routers coupled to the second memory device to influence a second color of the color display device.

8. (Previously Amended) The apparatus of claim 7 further comprising:

a third memory device; and

a third pair of repair routers coupled to the third memory device to influence a third color of the color display device.

9. (Currently Amended) A memory device comprising:

a plurality of addressable memory locations, each including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a repair router input data bus with a least significant bit and a plurality of non-least significant bits, and having a repair router output data bus coupled to the

plurality of addressable memory locations, the first repair router including routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the least significant bit of at least one of the plurality of addressable memory locations and to discard the least significant bit of the repair router input data bus.

10. (Original) The memory device of claim 9 wherein:

the plurality of addressable memory locations are arranged into a plurality of address ranges; and

the first repair router further includes address decoding circuitry to decode each of the plurality of address ranges.

11. (Original) The memory device of claim 10 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

12. (Original) The memory device of claim 9 wherein the first repair router is configured to route a specific non-least significant bit to the least significant bit of the plurality of addressable memory locations when a problem exists with the specific non-least significant bit in at least one of the plurality of addressable memory locations.

13. (Original) The memory device of claim 9 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

14. (Currently Amended) The memory device of claim 9 wherein:

the plurality of non-least significant bits of each of the addressable memory locations includes a next-to-least significant bit; and

the first repair router further includes routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the next-to-least significant bit of at least one of the plurality of addressable memory locations.

15. (Currently Amended) A display system comprising:

a display device having an array of pixels;

a memory having a plurality of addresses, each of the plurality of addresses corresponding to one pixel in the array of pixels, and each of the plurality of addresses including a least significant data bit and a plurality of non-least significant data bits; and

a first repair router to utilize the least significant data bit of at least one of the plurality of addresses to hold non-least significant information from any of the plurality of non-least significant data bits and to discard least significant information.

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16. (Original) The display system of claim 15 wherein the display device is a silicon light modulator.

17. (Original) The display system of claim 15 wherein the memory is configured to hold a first color information, the display system further comprising:

a second memory configured to hold second color information; and

a second repair router coupled to the second memory.

18. (Original) The display system of claim 17 further comprising:

a third memory configured to hold third color information; and

a third repair router coupled to the third memory.

19. (Currently Amended) The display system of claim 15 wherein:

the plurality of addresses are arranged in a plurality of groups; and

the first repair router includes routing circuitry to utilize the least significant bits of each of the plurality of groups separately.

20. (Currently Amended) An integrated circuit comprising:

a first memory device having an input data bus and an output data bus; ~~and~~

first and second repair routers coupled to the input data bus and the output data bus, respectively, the first and second repair routers including routing circuitry to route data to and from the first memory device as a function of defects in the first memory device; and

wherein the first and second repair routers include internal routing circuitry to utilize ~~any non-least significant bit of the memory device as~~ a least significant bit of the first memory device as a non-least significant bit and to discard least significant information.

21. (Currently Amended) The integrated circuit of claim 20 further comprising a reflective electrode coupled to the first memory device, the reflective electrode having a plurality of pixels responsive to data from the first memory device as received by the second repair router.

22. (Currently Amended) The integrated circuit of claim 21 wherein:

the first memory device includes a plurality of groups of data locations; and

the first and second repair routers each include circuitry to separately route data for each of the plurality of groups of data locations.

23. (Original) The integrated circuit of claim 22 further comprising:

second and third memory devices; and

second and third pairs of repair routers coupled to the second and third memory devices respectively.

Please add the following new claims:

24. (New) The apparatus of claim 2 wherein:

the first repair router further includes additional repair routing circuitry to discard a next-to-least significant bit of the first repair router input data bus.

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25. (New) The memory device of claim 14 wherein:

the first repair router further includes routing circuitry to discard a next-to-least significant bit of the repair router input data bus.